REMARKS/ARGUMENTS

Claims 1-23 are pending in this application. By this Amendment, Applicants amend claims 1-5, 7 11, 13-17, 19 and 23 and cancel claims 24-29.

Applicants affirm the election of Group I, including claims 1-23, without traverse.

Applicants note that the Examiner has not provided initialed and signed copies of the PTO-1449s which were submitted with two Information Disclosure Statements filed on January 22, 2004 and June 15, 2004. For the Examiner's convenience, Applicants submit herewith copies of the Information Disclosure Statements filed on January 22, 2004 and June 15, 2004 along with the stamped postcards which indicate that these Information Disclosure Statements were received by the USPTO. Applicants respectfully request that the Examiner include initialed and signed copies of the PTO-1449s which indicate that the Information Disclosure Statements have been entered and considered.

Claims 11 and 23 were rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite. Applicants have amended claims 11 and 23 to correct the informalities noted by the Examiner. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 1-5, 8-17 and 20-23 were rejected under 35 U.S.C. § 102(e) as being anticipated by Huang et al. (U.S. 2002/0180035). Claims 6 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang et al. in view of Punzalan et al. (U.S. 2003/0160309). Claims 7 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Huang et al. in view of Cheng et al. (U.S. 2003/0075812). Applicants respectfully traverse the rejections of claims 1-23.

Claim 1 has been amended to recite:

> "A process for manufacturing an integrated circuit package comprising:
> mounting a semiconductor die to a first surface of a substrate;
> mounting a die adapter to said semiconductor die;
> wire bonding said semiconductor die to ones of conductive traces

of said substrate;

mounting at least one collapsible spacer to at least one of a heat spreader, said die adapter and said substrate;

placing one of said heat spreader and said substrate on a surface of a lower mold die;

releasably clamping the other of said heat spreader and said substrate to an upper mold die, such that said collapsible spacer is disposed between said heat spreader and said substrate;

molding the semiconductor die, the substrate, the wire bonds, said die adapter, said at least one collapsible spacer and said heat spreader into a molding compound by molding in a mold cavity between said other of said heat spreader and said substrate and said surface of the lower mold die, to provide a molded package;

forming a ball grid array on a second surface of said substrate, bumps of said ball grid array being electrically connected to said conductive traces; and

singulating said integrated circuit package." (emphasis added)

Claim 13 recites features and method steps that are similar to the features and method steps recited in claim 1, including the above-emphasized features.

With the improved features and method steps of claims 1 and 13, including the steps of "placing one of said heat spreader and said substrate on a surface of a lower mold die," "releasably clamping the other of said heat spreader and said substrate to an upper mold die, such that said collapsible spacer is disposed between said heat spreader and said substrate" and "molding the semiconductor die, the substrate, the wire bonds, said die adapter, said at least one collapsible spacer and said heat spreader into a molding compound by molding in a mold cavity between said other of said heat spreader and said substrate and said surface of the lower mold die, to provide a molded package," Applicants have been able to provide a method for manufacturing an integrated circuit package in which a plurality of packages including heat spreaders can be manufactured in a single molded shot, and which produces an integrated circuit package having enhanced thermal characteristics (see, for example, paragraph [0002] on page 1 and paragraph [0011] on page 3 of the originally filed specification).

The Examiner alleged that Huang et al. teaches each and every feature and method step recited in Applicants' claims 1 and 13.

Claim 1 has been amended to recite the steps of "placing one of said heat spreader and said substrate on a surface of a lower mold die," "releasably clamping the other of said heat spreader and said substrate to an upper mold die, such that said collapsible spacer is disposed between said heat spreader and said substrate" and "molding the semiconductor die, the substrate, the wire bonds, said die adapter, said at least one collapsible spacer and said heat spreader into a molding compound by molding in a mold cavity between said other of said heat spreader and said substrate and said surface of the lower mold die, to provide a molded package," and claim 13 has been amended to recite similar method steps.

In contrast to Applicants' claims 1 and 13, Huang et al. specifically teaches that "[t]he structure of combining the heat sink module plate 23A, the chips 21 and the substrate module plate 20A is dimensioned for the gold layer 233A not contacting a top wall of a molded cavity of molds (not shown) but rather be properly spaced from the top wall, when the combined structure is placed in the mold cavity" (see paragraph [0035] on page 3 of Huang et al.). In other words, the heat sink module plate 23A (which the Examiner alleged corresponds to the heat spreader recited in Applicants' claims 1 and 13) is **neither** disposed on the surface of a lower mold die **nor** releasably clamped to an upper mold die, but rather, is disposed so as to be spaced from the top wall of a molded cavity of molds.

Thus, Huang et al. clearly fails to teach or suggest the steps of "placing one of said heat spreader and said substrate on a surface of a lower mold die," "releasably clamping the other of said heat spreader and said substrate to an upper mold die, such that said collapsible spacer is disposed between said heat spreader and said substrate" and "molding the semiconductor die, the substrate, the wire bonds, said die adapter, said at least one collapsible spacer and said heat spreader into a molding compound by molding in a mold cavity between said other of said heat spreader and said substrate

and said surface of the lower mold die, to provide a molded package" as recited in Applicants' claim 1, and similarly in Applicants' 13.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1 and 13 under 35 U.S.C. § 102(e) as being anticipated by Huang et al.

In anticipation of the Examiner changing the rejection of claims 1 and 13 to an obviousness rejection under 35 U.S.C. § 103(a) over Huang et al., the Examiner is reminded that it is error to find obviousness where references diverge and teach away from the invention at hand. W.L. Gore & Assoc. v. Garlock Inc., 220 USPQ 303, 311 (Fed. Cir. 1983). Since Huang et al. specifically discloses that the heat sink 23A **must** be spaced from a top wall of the mold cavity, Applicants respectfully submit that it would **not** have been obvious to modify the method of Huang et al. such that the heat sink 23A is disposed on a surface of a lower mold, or releasably clamped to an upper mold, because Huang et al. clearly teaches away from such modifications.

Punzalan et al. and Cheng et al. were relied upon to allegedly cure various deficiencies of Huang et al. However, neither Punzalan nor Cheng et al. teaches or suggests the steps of "placing one of said heat spreader and said substrate on a surface of a lower mold die," "releasably clamping the other of said heat spreader and said substrate to an upper mold die, such that said collapsible spacer is disposed between said heat spreader and said substrate" and "molding the semiconductor die, the substrate, the wire bonds, said die adapter, said at least one collapsible spacer and said heat spreader into a molding compound by molding in a mold cavity between said other of said heat spreader and said substrate and said surface of the lower mold die, to provide a molded package" as recited in Applicants' claims 1, and similarly in Applicants' claim 13. Thus, Applicants respectfully submit that Punzalan et al. and Cheng et al. fail to cure the deficiencies of Huang et al. described above.

Accordingly, Applicants respectfully submit that Huang et al., Punzalan et al. and Cheng et al., applied alone or in combination, fail to teach or suggest the unique

combination and arrangement of method steps and features recited in Applicants' claims 1 and 13.

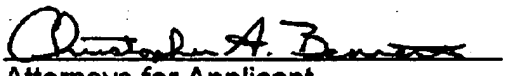
In view of the foregoing amendments and remarks, Applicants respectfully submit that Claims 1 and 13 are allowable. Claims 2-12 and 14-23 depend upon claims 1 and 13, and are therefore allowable for at least the reasons that claims 1 and 13 are allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: September 29, 2004



Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080

Serial No. 10/643,961 Attorney: CAS JRK Mailing Date 1/28/04
Client KN Our Ref. No. 50626 53
Title IMPROVED BALL GRID...
Applicant(s): Chun KO FAN et al
The following, due _____ in the U.S. Patent & Trademark Office, was received in the U.S. Patent & Trademark Office Mail Room on the date stamped hereon:

____ Patent Application, Including:
____ Pages of Specification, including:
____ Claims and Abstract
____ Drawings ____ Sheet(s)
____ Combined Decl./Power of Atty
____ Transmittal Letter
____ Associate Power of Attorney
____ Assignment with PTO 1595
____ Small Entity Status Form
____ Priority Document(s)
____ Petition for Extension of Time
____ Preliminary Amendment
✓ IDS w/ Form PTO 1449 w/ 24 cited references
____ Request for Continued Examination
____ Request for App. of Drwg. Corrections
✓ VIA HAND DELIVERY
✓ CERTIFICATE OF MAILING
____ EXPRESS MAIL NUMBER: _____

____ Amendment
____ Request for Reconsideration
____ Amendment After Final Rejection
____ Response to Restriction Requirement
____ Notice of Appeal
____ Letter to Official Draftsperson
____ Issue Fee Transmittal
____ Change of Address
____ Response to NTFMP
____ General Authorization to Charge Acct.
____ Charge Acct. Authorization for $_____
____ Credit Card Payment Form for $_____
____ Credit Card Payment Form for $_____
____ Check No. _____ for $_____
____ Check No. _____ for $_____
____ _____

OIPE JC1?? JAN 26 2004 PATENT & TRADEMARK OFFICE